



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/928,124	08/10/2001	John Snyder	14466	6453

25763 7590 04/23/2003

DORSEY & WHITNEY LLP
INTELLECTUAL PROPERTY DEPARTMENT
50 SOUTH SIXTH STREET
MINNEAPOLIS, MN 55402-1498

EXAMINER

PHAM, LONG

ART UNIT	PAPER NUMBER
----------	--------------

2814

DATE MAILED: 04/23/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.		Applicant(s)
	09/928,124		SNYDER ET AL. <i>fe</i>
	Examiner	Art Unit	
	Long Pham	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-108 is/are pending in the application.
- 4a) Of the above claim(s) 1-57 is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 58-108 is/are rejected.
- 7) ☐ Claim(s) ____ is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on ____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. ____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). ____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) ____ | 6) <input type="checkbox"/> Other: |

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of claims 58-108, species II in Paper No. 7 is acknowledged.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 58-78 are rejected under 35 U.S.C. 103(a) as being unpatentable over Koeneke et al. (US '550) in combination with Chooi et al. (US '080).

Koeneke et al. teach a method for manufacturing of MOSFET device, comprising:

providing a semiconductor substrate 20, fig. 2;

providing an electrically insulating layer 21 in contact with the substrate, fig. 2;

providing a gate electrode 24 in contact with at least a portion of the insulating layer, fig.2;

providing a source electrode 35 and a drain electrode 36 in contact with the substrate and proximal to the gate electrode wherein at least one of the source electrode and drain electrode forms a Schottky contact or Schottky-like region with the substrate, fig. 8 and associated text.

Koeneke et al. fail to teach that the electrically insulating layer or gate insulator has a dielectric constant greater than 15 or is made of ZrO_2 or HfO_2 as recited in present claims 58, 61, 65, 68, 72, and 75.

Chooi et al. teach that ZrO_2 or HfO_2 can be used as gate insulator material because of its stability on silicon surface. See col. 1, ln. 60 to col. 2, ln. 4.

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to use ZrO_2 or HfO_2 can be used as gate insulator material to obtain the above advantage.

With respect to claims 59, 60, 66, 67, 73, and 74, Koeneke et al. further teach that the source and drain electrodes are made of platinum silicide. See col. 6, ln. 5 and 6.

With respect to claims 62, 69, and 76, Koeneke et al. further teach that the Schottky source and drain electrodes are formed at least in areas adjacent to the channel. See fig. 8 and associated text.

With respect to claims 63, 70, and 77, Koeneke et al. further teach that an entire interface between at least one of the source and drain electrodes and the substrate forms a Schottky contact or Schottky-like region with substrate. See fig. 8 and associated text.

With respect to claims 64, 71, and 78, it is well-known that dopants are implanted into the channel region for adjusting threshold voltage of the MOSFET device.

3. Claims 79-108 are rejected under 35 U.S.C. 103(a) as being unpatentable over Koeneke et al. (US '550) in combination with Chooi et al. (US '080).

Koeneke et al. teach a method for manufacturing of MOSFET device, comprising:

providing a semiconductor substrate 20, fig. 2;

providing an electrically insulating layer 21 in contact with the substrate, fig. 2;
providing a gate electrode 24 in contact with at least a portion of the insulating layer, fig. 2;
exposing the substrate on one or more areas proximal to the gate electrode, fig. 6;
providing a thin film 34 of metal on at least a portion of the exposed substrate, fig. 7;
reacting the metal with the exposed substrate such that a Schottky or Schottky-like source electrode 35 and drain electrode 36 are formed on the substrate, fig. 8 and associated text.

Koeneke et al. fail to teach that the electrically insulating layer or gate insulator has a dielectric constant greater than 15 or is made of ZrO_2 or HfO_2 as recited in present claims 79, 85, 89, 95, 99, and 105.

Chooi et al. teach that ZrO_2 or HfO_2 can be used as gate insulator material because of its stability on silicon surface. See col. 1, ln. 60 to col. 2, ln. 4.

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to use ZrO_2 or HfO_2 can be used as gate insulator material to obtain the above advantage.

With respect to claims 81, 82, 91, 92, 101, and 102, Koeneke et al. further teach that reacting comprises of thermal annealing and that metal not reacted is removed. See col. 5, ln. 60 to col. 6, ln. 5.

Koeneke et al. fail to teach that a thin conducting film is formed on the insulating layer, the conducting film is patterned and etched to form the gate electrode, and a thin insulating layer is formed on the sidewalls of the gate electrode as recited in present claims 80, 90, and 100.

However, the above recited steps of forming a gate electrode is well-known to one of ordinary skill in the art of making semiconductor devices.

Art Unit: 2814

With respect to claims 83, 84, 93, 94, 103, and 104, Koeneke et al. further teach that the source and drain electrodes are made of platinum silicide. See col. 6, ln. 5 and 6.

With respect to claims 86, 96, and 106, Koeneke et al. further teach that the Schottky source and drain electrodes are formed at least in areas adjacent to the channel. See fig. 8 and associated text.

With respect to claims 87, 97, and 107 Koeneke et al. further teach that an entire interface between at least one of the source and drain electrodes and the substrate forms a Schottky contact or Schottky-like region with substrate. See fig. 8 and associated text.

With respect to claims 88, 98, and 108, it is well-known that dopants are implanted into the channel region for adjusting threshold voltage of the MOSFET device.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Long Pham whose telephone number is 703-308-1092. The examiner can normally be reached on M-F, 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on 703-308-4918. The fax phone numbers for the organization where this application or proceeding is assigned are 703-746-4082 for regular communications and 703-746-4082 for After Final communications.

Application/Control Number: 09/928,124
Art Unit: 2814

Page 6

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

A handwritten signature in black ink, appearing to read 'Long Pham', is written over the printed name.

Long Pham
Primary Examiner
Art Unit 2814

L. P.
April 19, 2003